

Convert 1 to 5V signal to 4- to 20-mA output

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Despite the long-predicted demise of the 4- to 20-mA current loop, this analog interface is still the most common method of connecting current-loop sources to a sensing circuit. This interface requires the conversion of a voltage signal—typically, 1 to 5V—to a 4- to 20-mA output. Stringent accuracy requirements dictate the use of either expensive precision resistors or a trimming potentiometer to calibrate out the initial error of less precise devices to meet the design goals.

Neither technique is optimal in today's surface-mounted, automatic-test-equipment-driven production environment. It's difficult to get precise resistors in surface-mount packages, and trimming potentiometers require human intervention, a requirement that is incompatible with production goals.

The Linear Technology [LT5400](#) quad matched resistor network helps to solve these issues in a simple circuit that requires no trim adjustments but achieves a total error of less than 0.2% (**Figure 1**). The circuit uses two amplifier stages to exploit the unique matching characteristics of the [LT5400](#). The first stage applies a 1 to 5V output—typically, from a DAC—to the noninverting input of op amp IC_{1A} . This voltage sets the current through R_1 to exactly V_{IN}/R_1 through FET Q_2 . The same current is pulled down through R_2 , so the voltage at the bottom of R_2 is the 24V loop supply minus the input voltage.

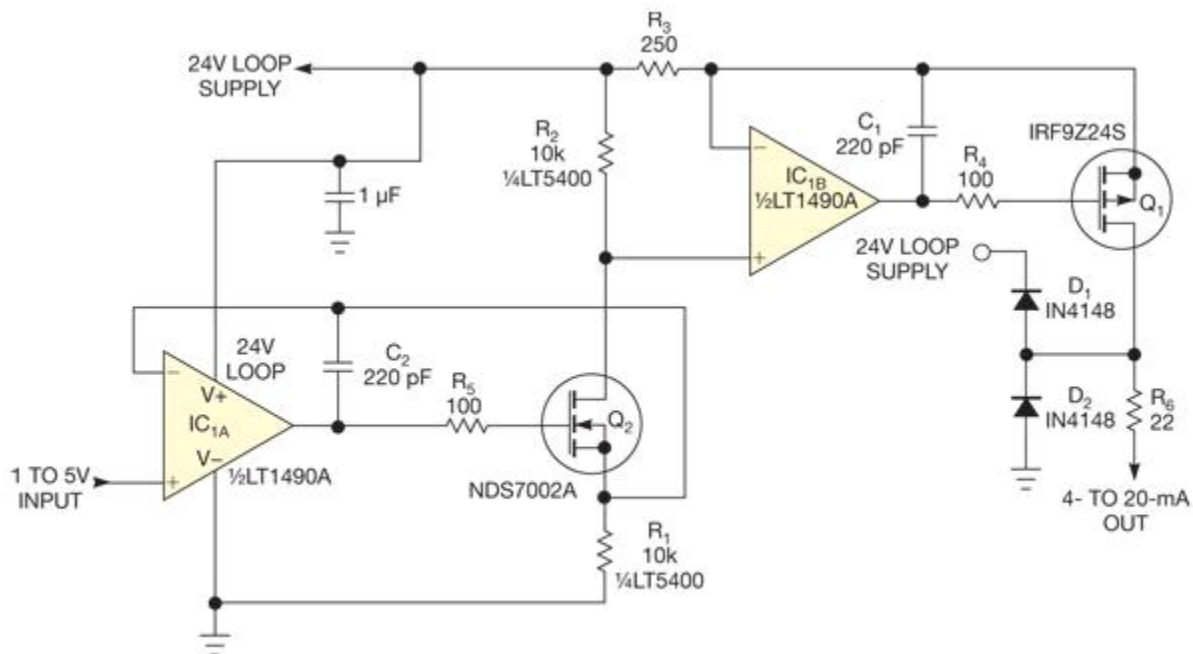


Figure 1 Precision matched resistors provide accurate voltage-to-current conversion.

This portion of the circuit has three main error sources: the matching of R_1 and R_2 , IC_{1A} 's offset voltage, and Q_2 's leakage. The exact values of R_1 and R_2 are not critical, but they must exactly match each other. The [LT5400A](#) grade achieves this goal with $\pm 0.01\%$ error. The [LT1490A](#) has less-than-700- μV offset voltage over 0 to 70°C. This voltage contributes 0.07% error at an input voltage of 1V. The [NDS7002A](#) has a leakage current of 10 nA, although it is usually much less. This leakage current represents an error of 0.001%.

The second stage holds the voltage on R_3 equal to the voltage on R_2 by pulling current through Q_1 . Because the voltage across R_2 equals the input voltage, the current through Q_1 is exactly the input voltage divided by R_3 . By using a precision 250 Ω current shunt for R_3 , the current accurately tracks the input voltage.

The error sources for the second stage are R_3 's value, IC_{1B} 's offset voltage, and Q_1 's leakage current. Resistor R_3 directly sets the output current, so its value is crucial to the precision of the circuit. This circuit takes advantage of the commonly used 250 Ω current-loop-completion shunt resistor. The Riedon SF-2 part in the **figure** has 0.1% initial accuracy and low temperature drift. As in the first stage, offset voltage contributes no more than 0.07% error. Q_1 has less than 100-nA leakage, yielding a maximum error of 0.0025%.



Total output error is better than 0.2% without any trimming. Current-sensing resistor R_3 is the dominant source of error. If you use a higher-quality device, such as the Vishay PLT series, you can achieve an accuracy of 0.1%. Current-loop outputs are subject to considerable stresses in use. Diodes D_1 and D_2 from the output to the 24V loop supply and ground help protect Q_1 ; R_6 provides some isolation. You can achieve more isolation by increasing the value of R_6 , with the trade-off of some compliance voltage at the output. If the maximum output-voltage requirement is less than 10V, you can increase R_6 's value to 100 Ω , affording even more isolation from output stress. If your design requires increased protection, you can fit a transient-voltage suppressor to the output with some loss of accuracy due to leakage current.

This design uses only two of the four matched resistors in the [LT5400](#) package. You can use the other two for other circuit functions, such as a precision inverter, or another 4- to 20-mA converter. Alternatively, you can place the other resistors in parallel with R_1 and R_2 . This approach lowers the resistor's statistical error contribution by the square root of two.